Amendments to the Specification:

Please replace the paragraph beginning at page 8, line 2, with the following rewritten paragraph:

Referring now to Figure 1, in accordance with the preferred embodiment of the invention, processor 100 generally comprises a fetch unit 101, a branch predictor 102, a multiplexer 104, an instruction cache 106, a register map 108, an issue queue 110, a register file 112, an execution unit 114, an L1 cache 116~~16~~, an L2 cache 118, a victim buffer 120 and a miss address file 122. Other components (not specifically shown) or different components can be provided as desired. Further, one or more of the components shown in Figure 1 can be implemented as a plurality of such components. For example, there may be more than one branch predictor 102, register map 108, issue queue 110, register file 112, execution unit 114, victim buffer 120 and miss address file 122. Additional such components may be provided to permit concurrent processing of multiple instructions through the processor. Further, a set of components 108-114 can be provided to process integer-type instructions and another set to process floating point-type instructions.

Please replace the Abstract with the following rewritten Abstract:

ABSTRACT

~~The problems noted above are solved in large part by a computer system having one or more processors. Each processor has a branch predictor which dynamically predicts each conditional branch instruction. Software written for the processors to execute includes static branch prediction instructions embedded in the software. Each branch prediction instruction includes a pair of predictor bits that corresponds to another instruction which may be a conditional branch instruction. The pair of bits encodes whether, assuming the corresponding instruction is a branch, the branch is predicted as taken or not taken. This information encoded in the branch prediction instruction overrides the dynamic branch predictor in the processor. If the corresponding instruction is not a branch~~